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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/604,414	07/18/2003	Darren Lane Anand	BUR920020093US1	1413

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EXAMINER	
BARAN, MARY C	

ART UNIT	PAPER NUMBER
2857	

DATE MAILED: 02/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/604,414	ANAND ET AL.	
	Examiner	Art Unit	
	Mary Kate B. Baran	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 5-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 5-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The action is responsive to the Amendment filed on 9 January 2006. Claims 1 and 5-20 are pending.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1 and 5-20 are rejected under 35 U.S.C. 102(a) as being anticipated by Cowan et al. ("On-chip Repair and an ATE Independent Fusing Methodology") (hereinafter Cowan).

Referring to claim 1, Cowan teaches a circuit for programming and testing electrical fuse circuits in a device (see Cowan, page 178, "Introduction" column 2 paragraph 1 lines 1-14), said circuit comprising: an efuse circuit that includes a fuse, a blow device, and a control input for said blow device (see Cowan, page 179 Figure 1); a first circuit capable of determining when to blow said fuse (see Cowan, page 179 "The e-fuse" column 1 paragraph 2 lines 2-9).

Cowan further teaches that said first logic means comprises: a first latch component having multiple inputs and which provides a true output (see Cowan, page 179 Figure 1 "Fuse Latch"); a second latch component having multiple inputs and which

provides both a second true output and a complement output (see Cowan, page 179 Figure 1 "Program Latch"); wherein said second latch component is programmed with a blow value for said fuse such that the blow value dictates when a fuse is to be blown (see Cowan, page 179 "The e-fuse" column 2 paragraph 2 lines 2-9); and a EFUSEPROGRAM signal that together with said true output and said second true output provides the control input to said blow device (see Cowan, page 179 "The e-fuse" column 2 paragraph 2 lines 9-13).

Cowan further teaches a second logic means capable of triggering a bypass of a pre-blow process within said efuse circuit when said fuse is not to be blown, wherein a shifted 1 propagating through a plurality of efuse circuits within said device is passed to a next downstream efuse circuit without delay attributable to said pre-blow process (see Cowan, page 179 "The e-fuse" column 2 paragraph 2 lines 2-9); wherein said second logic means comprises: comprises an AND gate having a first input coupled to said complement output of said second latch, a second input coupled to said program signal, and a result output; a multiplexer (MUX) having a first MUX input coupled to the true output of said first latch component, a second MUX input coupled to a selected output of a previous MUX of a third efuse circuit sequentially before said efuse circuit, a select input coupled to said result output of said AND gate, and a select output (see Cowan, page 179 Figure 1; and third logic means for maintaining the EFUSEPROGRAM signal in a logic low state during serial readout of fuse latches within a shift path, such that the MUX is forced to choose the input from a fuse latch of the circuit and the fuse latch is

forced to be within the shift path regardless of the state of the pattern latch (see Cowan, page 179 column 2 paragraph 1 lines 1-11).

Referring to claim 5, Cowan teaches that said first MUX input is selected when said result output is low (0) (see Cowan, page 179 "The e-fuse" column 2 paragraph 1 lines 1-4); said second MUX input is selected when said result output is high (1) (see Cowan, page 179 "The e-fuse" column 2 paragraph 1 lines 4-6); and said blow device is triggered to blow said fuse when said first MUX input is selected and both said true output and said second true output are high (see Cowan, page 179 "The e-fuse" column 2 paragraph 2 lines 13-16).

Referring to claim 6, Cowan teaches a device that includes multiple, serially connected, electrical fuse circuits, a system for programming and testing efuse circuits (see Cowan, page 180 Figure 2), said system comprising: an AND gate having two inputs and a result output (see Cowan, page 179 Figure 1); a multiplexer (MUX) having a first input, a second input, a select input, and a MUX output, wherein select input is coupled to said result output of said AND gate (see Cowan, page 179 Figure 1 "'Look-ahead' mux"); wherein, said efuse circuit includes a fuse coupled to a switch that is controlled by signals from a fuse latch, a pattern latch, and a program signal source (see Cowan, page 179 Figure 1), said pattern latch being programmed with a fuse blow status indicating whether of not said fuse is to be blown during device testing (see Cowan, page 179 "The e-fuse" column 2 paragraph 2 lines 2-9).

Cowan further teaches a first logic means for determining when to blow said fuse, wherein said first logic means comprises an EFUSEPROGRAM signal that together with said true output and said second true output provides the control input to said blow device (see Cowan, page 179 "The e-fuse" column 2 paragraph 2 lines 9-13); second logic means for enabling a bypass of a pre-blow process within said efuse circuit when said fuse blow status indicates that said fuse is not to be blown, such that a time delay associated with said fuse-blow process is substantially eliminated as a testing operation proceeds to each efuse circuit within said device (see Cowan, page 179 "The e-fuse" column 2 paragraph 2 lines 2-9); and third logic means for maintaining the EFUSEPROGRAM signal in a logic low state during serial readout of fuse latches within a shift path, such that the MUX is forced to choose the input from a fuse latch of the circuit and the fuse latch is forced to be within the shift path regardless of the state of the pattern latch (see Cowan, page 179 column 2 paragraph 1 lines 1-11).

Referring to claim 7, Cowan teaches that said enabling circuit includes connecting components and signals of said efuse circuit to said MUX and said AND gate, wherein said MUC and said AND gate provide a bypass function that determines when a shifter "1" that is being serially propagated to each of said efuse circuits should be forwarded to said fuse latch for initiating a blow of said fuse, wherein when a fuse blow status within said pattern latch indicates that said fuse is not to be blown, said MUX forwards said shifted 1 to a next efuse circuit without waiting on a completion of

said pre-blow process (see Cowan, page 179 "The e-fuse" column 2 paragraph 2 lines 1-16).

Referring to claim 8, Cowan teaches that a first input of said AND gate is coupled to a complement of a signal from said pattern latch indicating the fuse blow status (see Cowan, page 179 Figure 1); a second input of said AND logic is coupled to said program signal source (see Cowan, page 179 Figure 1); said first input of said MUX is coupled to said fuse latch; and said second input of said MUX is coupled to a MUX output of a previous MUX (see Cowan, page 179 Figure 1 "'Look-ahead' mux").

Referring to claim 9, Cowan teaches that further said MUX output of said MUX is connected to a second input of a next MUX of a next efuse circuit (see Cowan, page 179 Figure 1 "'Look-ahead' mux").

Referring to claim 10, Cowan teaches that said second input of said MUX is coupled to a fuse in signal when said MUX is a first MUX in said serially connected efuse circuits (see Cowan, page 179 Figure 1 "Fuse Data/Fuse Sequence Control").

Referring to claim 11, Cowan teaches that said efuse circuit is a first efuse circuit that is serially connected to a second efuse circuit, whose fuse blow status indicates its fuse should not be blown, and a third efuse circuit whose fuse blow status indicates its fuse should be blown (see Cowan, page 180 Figure 2 "Fuse PSR"), said circuit

comprising: a routing circuit capable of routing said shifted 1 through said fuse latch of said first efuse circuit, subsequently bypassing a fuse latch of said second efuse circuit, and then routing said shifted 1 through a fuse latch of said third efuse circuit, wherein only said first efuse circuit and said third efuse circuit utilizes processing time for routing said shifted 1 through respective fuse latches before forwarding said shifted 1 to a next efuse circuit (see Cowan, page 179 "The e-fuse" column 2 paragraph 2 lines 1-16).

Referring to claim 12, Cowan teaches a device that includes multiple, serially connected efuse circuits (see Cowan, page 180 Figure 2), each having a fuse, a fuse switch, a fuse latch, a pattern latch, a fuse program signal, AND logic and a bypass multiplexer (MUX) (see Cowan, page 179 Figure 1), a method for reducing programming and test time for said device comprising: storing a fuse blow status within said pattern latch (see Cowan, page 179 "The e-fuse" column 2 paragraph 2 lines 1-4); ANDing a complement of said fuse blow status with said fuse program signal (see Cowan, page 179 Figure 1 "Program Latch"); selecting one of two inputs of said MUX based on a result of said ANDing step, said inputs including a first input coupled to a true output of said fuse latch and a second input coupled to a MUX output of a previous efuse circuit (see Cowan, page 179 Figure 1 "'Look-ahead' mux"); forwarding a shifted 1 propagating through said device to a next efuse circuit without waiting for a pre-blow processing time to elapse when said second input is selected, wherein a time delay for propagating said shifted 1 through said efuse circuit is substantially eliminated (see Cowan, page 179 "The e-fuse" column 2 paragraph 2 lines 2-9).

Cowan further teaches determining when to blow said fuse, wherein said first logic means comprises an EFUSEPROGRAM signal that together with said true output and said second true output provides the control input to said blow device (see Cowan, page 179 "The e-fuse" column 2 paragraph 2 lines 9-13); and maintaining the EFUSEPROGRAM signal in a logic low state during serial readout of fuse latches within a shift path, such that the MUX is forced to choose the input from a fuse latch of the circuit and the fuse latch is forced to be within the shift path regardless of the state of the pattern latch (see Cowan, page 179 column 2 paragraph 1 lines 1-11).

Referring to claims 13, 16 and 19, Cowan further teaches that the pattern latch register controls an effective length of the fuse latch register to equal a number of logic high states (1) onset latches in the pattern register only when EFUSEPROGRAM is at a logic high state (see Cowan, page 183 column 1 lines 4-14).

Referring to claims 14 and 17, Cowan further teaches that a fuse blow process is indicated for an eFuse circuit if the MUX selects the fuse latch input, and the fuse blow process is completed before the shifted 1 is passed to the next eFuse circuit (see Cowan, page 179 paragraph 2 lines 1-16).

Referring to claims 15 and 18, Cowan teaches that when the MUX does not select the fuse latch input, the MUX bypass input is selected and the shifted 1 is sent to the next eFuse circuit (see Cowan, page 179 paragraph 2 lines 1-9).

Referring to claim 20, Cowan teaches that a fuse blow process is indicated for an eFuse circuit if the MUX selects the fuse latch input, and the fuse blow process is completed before the shifted 1 is passed to the next eFuse circuit (see Cowan, page 179 paragraph 2 lines 1-16); and when the MUX does not select the fuse latch input, the MUX bypass input is selected and the shifted 1 is sent to the next eFuse circuit (see Cowan, page 179 paragraph 2 lines 1-9).

Response to Arguments

3. Applicant's arguments filed 9 January 2006 have been fully considered but they are not persuasive.

Applicant argues that the Cowan et al. reference is not valid under 35 U.S.C. 102(a). However, Applicant's arguments are not well taken. While there are two common inventors/authors, Ouellette and Oakland, both the application and the reference list additional inventors and authors, therefore the Cowan et al. reference is still valid under 35 U.S.C. 102(a). Applicant is asked to file 37 C.F.R. 1.132 Affidavits for each co-author not listed on the application, add the additional authors as inventors, or amend to overcome the prior art.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mary Kate B. Baran whose telephone number is (571)

272-2211. The examiner can normally be reached on Monday - Friday from 9:00 am to 6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached on (571) 272-2216. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

5 February 2006

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